REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

The claims have been amended to correct a typographical error.

Claims 1 and 2 stand rejected under 35 U.S.C. 102(b) as being anticipated by Gaytan et al. (US 5,638,367).

Referring first to FIG. 4 of the subject patent application, it is noted that his system includes (1) a sampling register; (2) a shifter for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets; (3) an accumulator register for storing the shifted bytes; (4) a staging register for storing the bytes stored in the accumulator register; and (5) a multiplexer coupled to the accumulator register and the staging register. To put it in still another way, Applicant stores in sampling register 600, then FIRST SHIFTS in shifter 602, then sends the SHIFTED data to an accumulator 604 and staging register 606 with the SHIFTED data in the accumulator 604 being fed directly to one input of a multiplexer 608 and the SHIFTED data in the staging register 606 being fed to a second input of the multiplexer 608. Such an arrangement is not described in Gaytan et al. (US 5,638,367).

The Examiner states that the Gaytan et al. system comprises:

> a sampling register (fig. 1, fig. 3 and fig. 6a, i.e. there must be a register between host memory 395 and word packing circuit 600 in fig. 3) having W byte locations for storing W bytes read from a selected one of the word-based locations of the memory, such read bytes being bytes of a currently gathered one of the packets (col. 6, lines 34-44);
>
> a shifter (fig. 6a, el. 610 and 615) for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets (col. 6, lines 53-65);
>
> an accumulator register (fig. 6b, el. 660) having W byte locations for storing the shifted bytes in response to a clock pulse (col. 9, lines 43-44);
>
> a staging register (fig. 6b, el. 665) having W byte locations, for storing

the bytes stored in the accumulator register in response to a subsequent clock pulse (col. 9, lines 44-47); and

a multiplexer (fig. 6b, el. 675) having a W sections, each of the W sections being coupled to a corresponding one of the W byte locations of the accumulator register and a corresponding one of the W byte locations of the staging register, each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior gathered ones of the packets and the number of bytes being gathered from the currently gathered one of the packets (col. 9, lines 31-67 and col. 10, lines 25-30) to provide at an output of the multiplexer bytes to be transmitted as the transmitted block of data having the selected portions appended contiguously one to the other (fig 1 and fig. 7a-7i).

It is respectfully submitted that a elements 610 and 615 of Gaytan et al. (US 5,638,367) DO NOT shift the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets (col. 6, lines 53-65) BUT RATHER selects different portions of the word. As stated in col. 6, lines 53-65:

As shown, the lower data word is transferred into (i) the latch element 605, (ii) a first port of the first input selector 610 and (iii) a first port of the input second selector 615 during a first transfer cycle. The upper data word is input into a second port of the second input selector 610. <u>These first and second input selectors 610 and 615 are configured to be disabled to prevent an invalid word (32-bits) from being written into the read storage element 620</u> by setting Select1 equal to logic "1" and Select0 equal to the value of bit 2 of the starting address of valid data within an associated TX data buffer of the host memory. It is contemplated that the configuration of the Select0,1 lines can be deduced for all sizes of the system bus (e.g., "00" for 32-bit system bus). (emphasis added)

Thus, it is respectfully submitted that a elements 610 and 615 of Gaytan et al. (US 5,638,367) DO NOT shift the bytes stored in the sampling register. It is noted that Gaytan et al. (US 5,638,367) describes element 655 as a byte rotation circuit and such circuit is DOWNSTREAM of element 660 and register 665.

Thus, as noted above, applicant points out that his system includes (1) a <u>sampling</u>

register; (2) a shifter for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets; (3) an accumulator register for storing the shifted bytes; (4) a staging register for storing the bytes stored in the accumulator register; and (5) a multiplexer coupled to the accumulator register and the staging register. Such an arrangement is not described in Gaytan et al. (US 5,638,367).

To put it in still another way, Applicant stores in sampling register 600, then FIRST SHIFTS in shifter 602, then sends the SHIFTED data to an accumulator 604 and staging register 606 with the SHIFTED data in the accumulator 604 being fed directly to one input of a multiplexer 608 and the SHIFTED data in the staging register 606 being fed to a second input of the multiplexer 608. Such an arrangement is not described in Gaytan et al. (US 5,638,367).

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

October 31. 2007
Date

/richard sharkansky/
Richard M. Sharkansky Reg. No.: 25,800
Attorney for Applicant(s)
P. O. Box 557
Telephone: (508) 477-4311
Facsimile: (508) 477-7234